

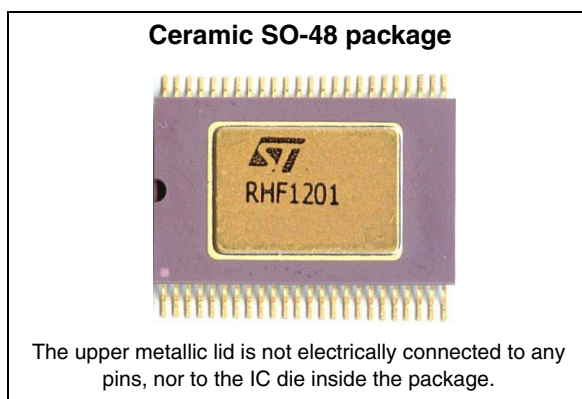
Rad-hard 12-bit 50 Msp/s A/D converter

Features

- Qml-V qualified, smd 5962-05217
- Rad hard: 300 kRad(Si) TID
- Failure immune (SEFI) and latchup immune (SEL) up to 120 MeV-cm²/mg at 2.7 V and 125° C
- Hermetic package
- Wide sampling range
- Tested at 50 Msp/s
- Optimwatt™ adaptive power:
44 mW at 0.5 Msp/s, 100 mW at 50 Msp/s
- Optimized for 2 V_{pp} differential input
- SFDR up to 75 dB at F_S = 50 Msp/s,
F_{in} = 15 MHz
- 2.5 V/3.3 V compatible digital I/O
- Built-in reference voltage with external bias capability

Applications

- Digital communication satellites
- Space data acquisition systems
- Aerospace instrumentation
- Nuclear and high-energy physics



Description

The RHF1201 is a 12-bit 50 Msp/s sampling frequency analog-to-digital converter that uses pure (ELDRS-free) CMOS 0.25 μm technology combining high performance, radiation robustness and very low power consumption. The device is based on a pipeline structure and digital error correction to provide excellent static linearity. Specifically designed to optimize the speed power consumption ratio, the RHF1201 integrates a proprietary track-and-hold structure making it ideal for IF-sampling applications up to 150 MHz. A voltage reference network is integrated in the circuit to simplify the design and minimize external components. A tri-state capability is available on the outputs to allow common bus sharing. Output data can be coded in two different formats. A Data Ready signal, raised when the data is valid on the output, can be used for synchronization purposes.

Table 1. Device summary

Order code ⁽¹⁾	SMD pin	Quality level	Package	Lead finish	Packing	Marking	EPPL
RHF1201KSO1	-	Engineering model	SO-48	Gold	Strip pack	RHF1201KSO1	-
RHF1201KSO-01V	5962F0521701VXC	QMLV-Flight	SO-48	Gold	Strip pack	5962F0521701VXC	-

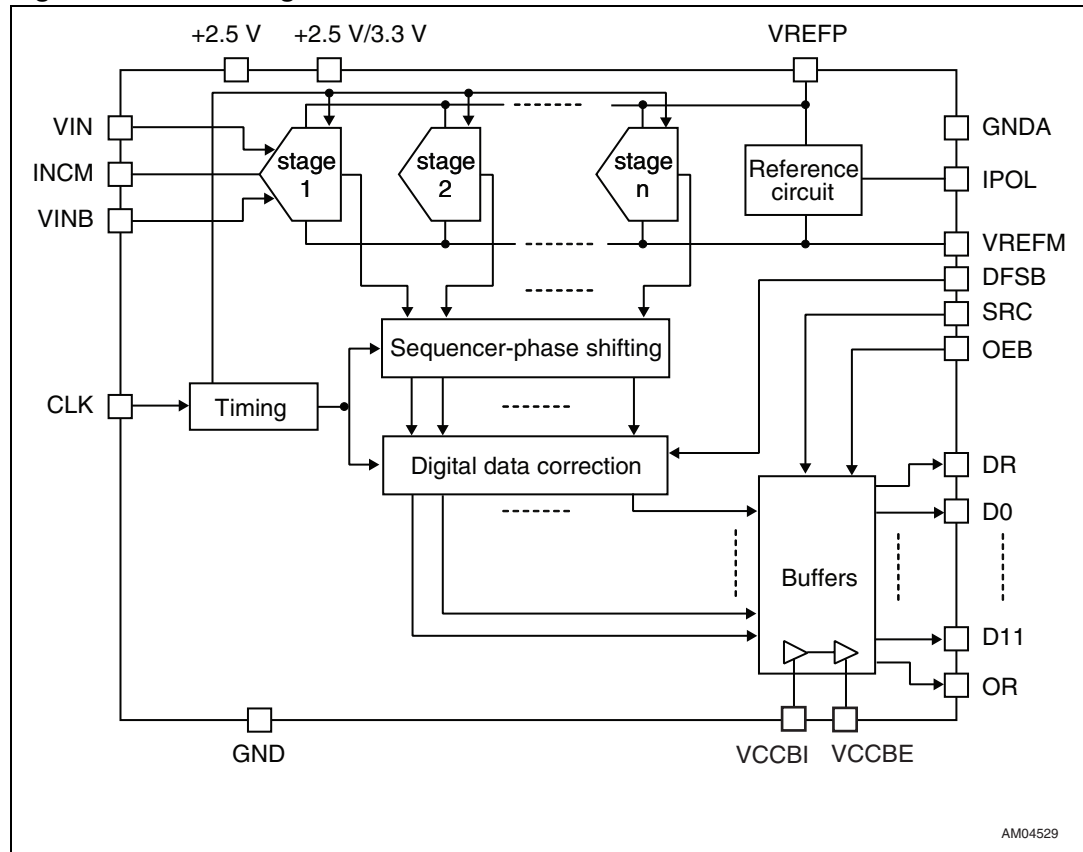
1. Contact your ST sales office for information about the specific conditions for products in die form and for information about SMD packages.

Contents

1	Block diagram	3
2	Pin connections	4
3	Pin descriptions	5
4	Equivalent circuits	6
5	Timing characteristics	8
6	Absolute maximum ratings and operating conditions	9
7	Electrical characteristics (unchanged after 300 kRad)	10
7.1	RHF1201 operating modes	19
7.1.1	Inputs	19
7.1.2	Outputs	20
7.2	Driving the analog input	21
7.3	Reference connection	25
7.3.1	Internal reference	25
7.3.2	External reference	25
7.4	Clock input	26
7.5	Power consumption optimization	27
7.6	Layout precautions	28
8	Definitions of specified parameters	29
8.1	Static parameters	29
8.2	Dynamic parameters	29
9	Package information	31
10	Revision history	33

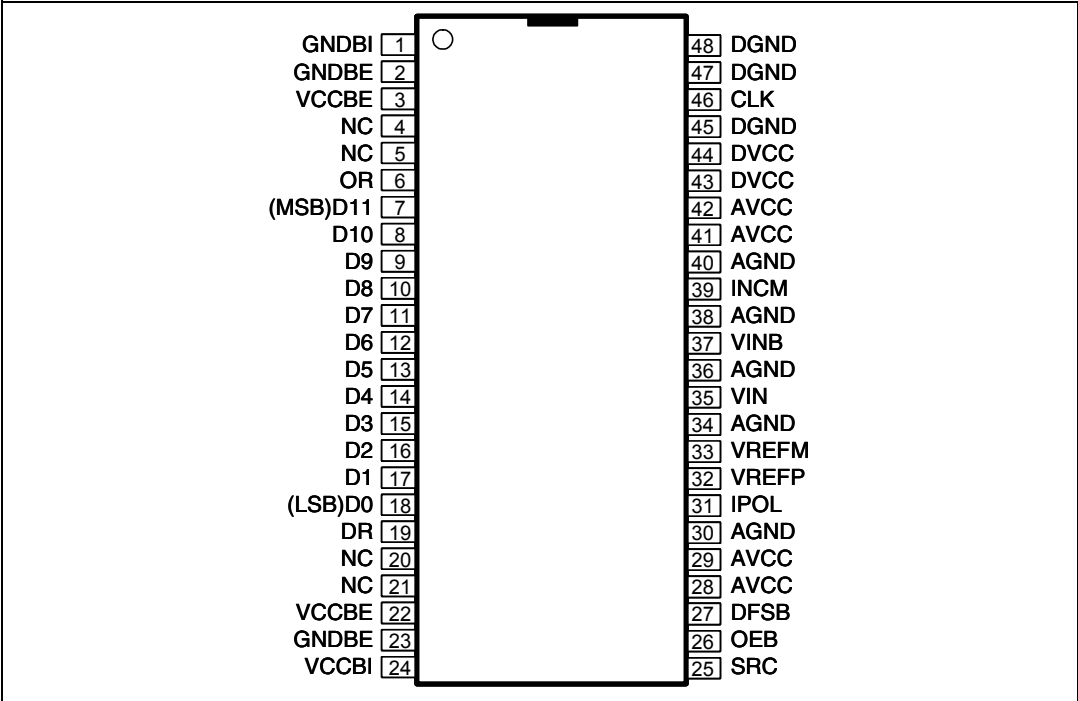
1 Block diagram

Figure 1. Block diagram



2 Pin connections

Figure 2. Pin connections (top view)



3 Pin descriptions

Table 2. Pin descriptions

Pin	Name	Description	Note	Pin	Name	Description	Note
1	GNDBI	Digital buffer ground	0 V	25	SRC	Slew rate control input	2.5 V/3.3 V CMOS input
2	GNDBE	Digital buffer ground	0 V	26	OEB	Output Enable input	2.5 V/3.3 V CMOS input
3	VCCBE	Digital buffer power supply	2.5 V/3.3 V	27	DFSB	Data Format Select input	2.5 V/3.3 V CMOS input
4		NC	Not connected to the dice	28	AVCC	Analog power supply	2.5 V
5		NC	Not connected to the dice	29	AVCC	Analog power supply	2.5 V
6	OR	Out-of-range output	CMOS output (2.5 V/3.3 V)	30	AGND	Analog ground	0 V
7	D11(MSB)	Most significant bit output	CMOS output (2.5 V/3.3 V)	31	IPOL	Analog bias current input	
8	D10	Digital output	CMOS output (2.5 V/3.3 V)	32	VREFP	Top voltage reference	Can be internal or external
9	D9	Digital output	CMOS output (2.5 V/3.3 V)	33	VREFM	Bottom voltage reference	External
10	D8	Digital output	CMOS output (2.5 V/3.3 V)	34	AGND	Analog ground	0 V
11	D7	Digital output	CMOS output (2.5 V/3.3 V)	35	VIN	Analog input	Optimized for 1V _{pp}
12	D6	Digital output	CMOS output (2.5 V/3.3 V)	36	AGND	Analog ground	0 V
13	D5	Digital output	CMOS output (2.5 V/3.3 V)	37	VINB	Inverted analog input	Optimized for 1V _{pp}
14	D4	Digital output	CMOS output (2.5 V/3.3 V)	38	AGND	Analog ground	0 V
15	D3	Digital output	CMOS output (2.5 V/3.3 V)	39	INCM	Input common mode	Can be internal or external
16	D2	Digital output	CMOS output (2.5 V/3.3 V)	40	AGND	Analog ground	0 V
17	D1	Digital output	CMOS output (2.5 V/3.3 V)	41	AVCC	Analog power supply	2.5 V
18	D0(LSB)	Least significant bit output	CMOS output (2.5 V/3.3 V)	42	AVCC	Analog power supply	2.5 V
19	DR	Data ready output	CMOS output (2.5 V/3.3 V)	43	DVCC	Digital power supply	2.5 V
20		NC	Not connected to the dice	44	DVCC	Digital power supply	2.5 V
21		NC	Not connected to the dice	45	DGND	Digital ground	0 V
22	VCCBE	Digital buffer power supply	2.5 V/3.3 V	46	CLK	Clock input	2.5 V compatible CMOS input
23	GNDBE	Digital buffer ground	0 V	47	DGND	Digital ground	0 V
24	VCCBI	Digital buffer power supply	2.5 V	48	DGND	Digital ground	0 V

4 Equivalent circuits

Figure 3. Analog inputs

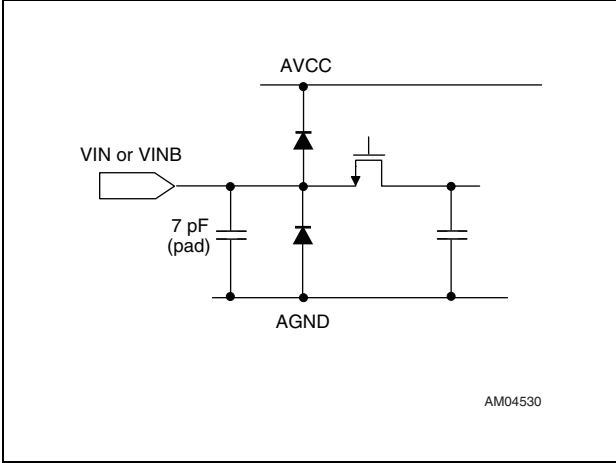


Figure 4. Output buffers

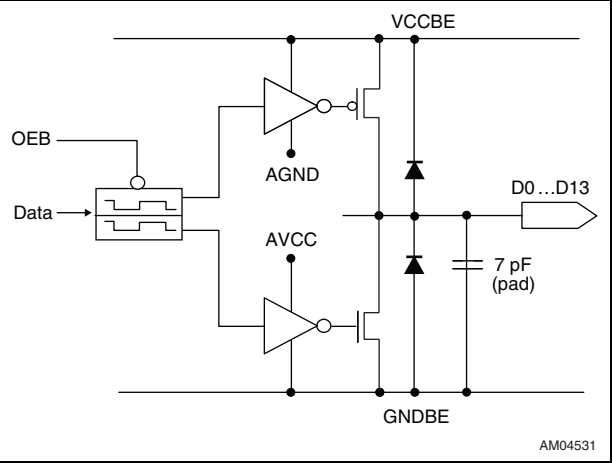


Figure 5. Clock input

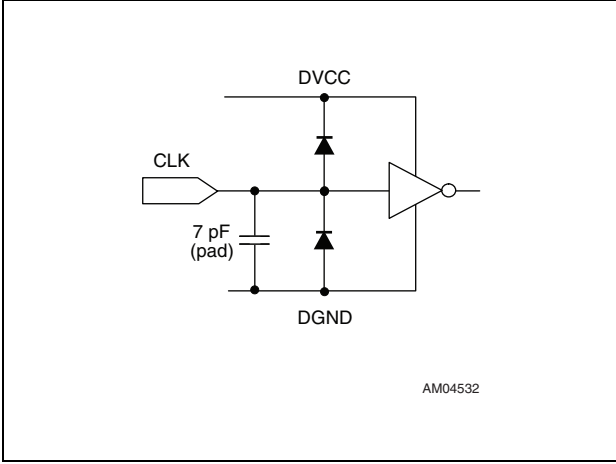


Figure 6. Data format input

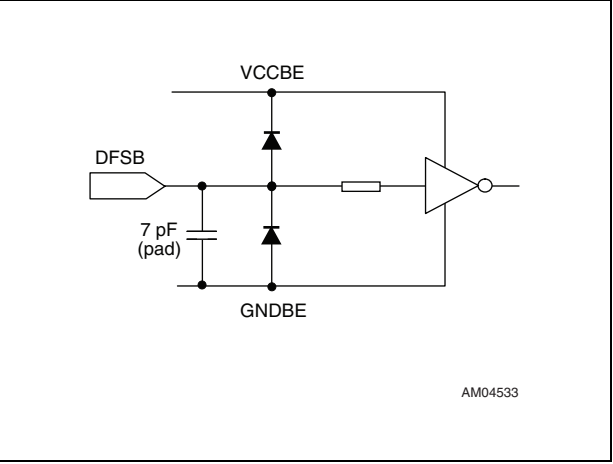


Figure 7. Slew rate control input

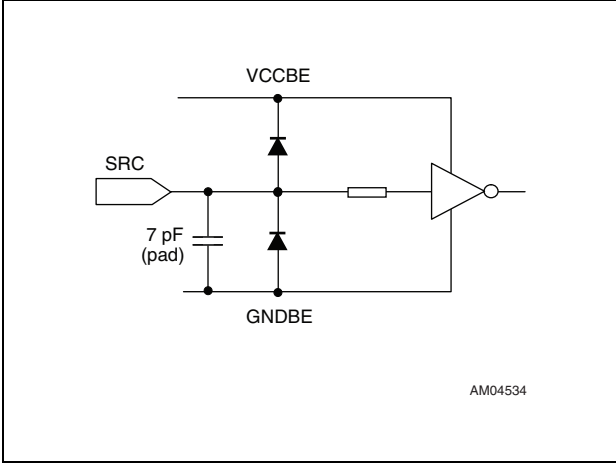


Figure 8. Output enable input

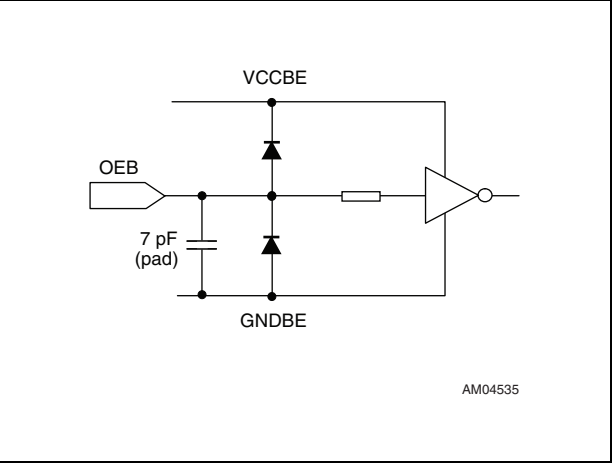


Figure 9. VREFP and INCM input

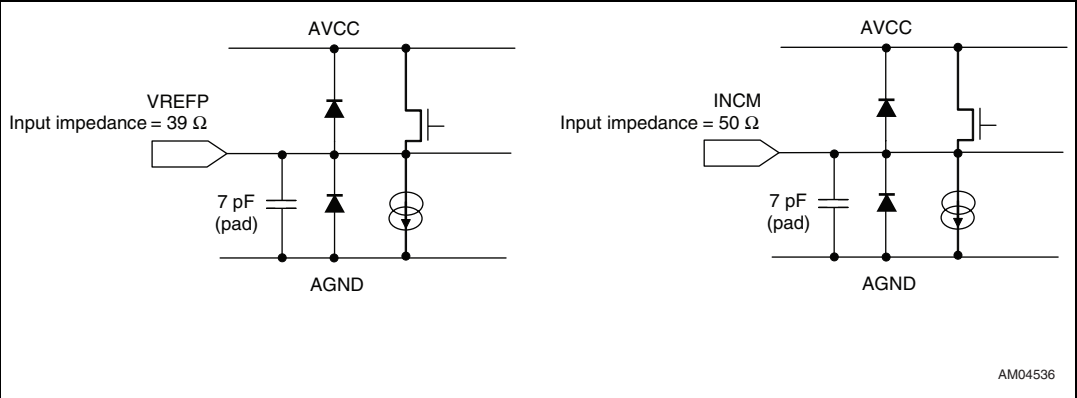
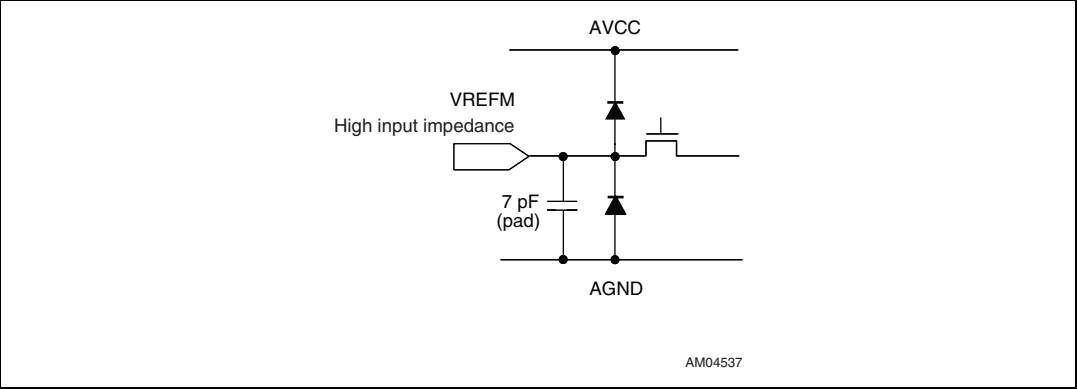


Figure 10. VREFM input



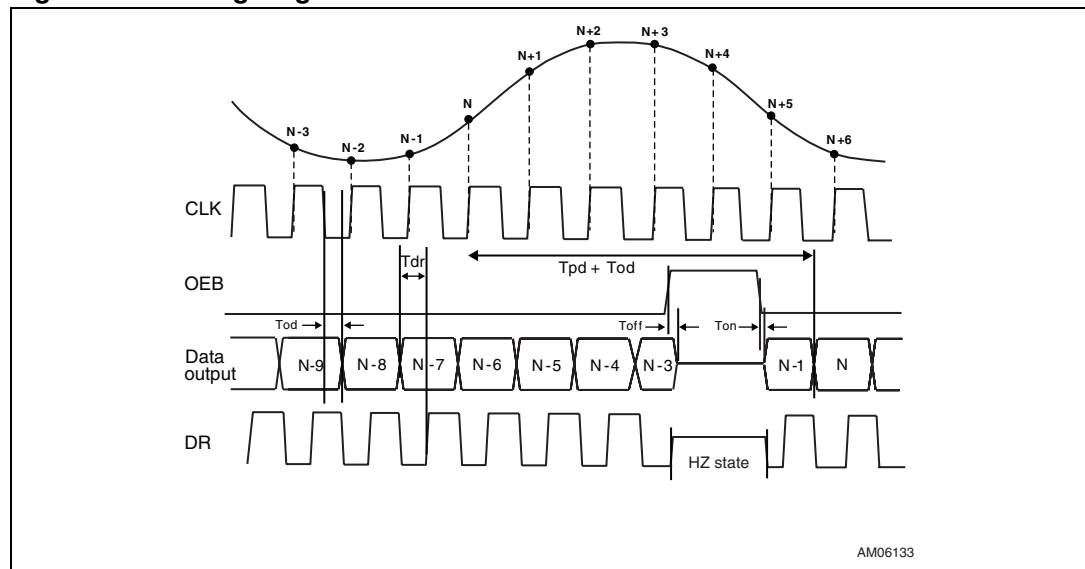
5 Timing characteristics

Table 3. Timing table

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
DC	Clock duty cycle ⁽¹⁾	$F_S = 45 \text{ Msps}$	45	50	65	%
T_{od}	Data output delay ⁽²⁾ (fall of clock to data valid)	10 pF load	4	5	6	ns
T_{pd}	Data pipeline delay ⁽²⁾		5.5	5.5	5.5	cycles
T_{dr}	Data ready rising edge delay after data change ⁽³⁾	Duty cycle = 50%		0.5		cycles
T_{on}	Falling edge of OEB to digital output valid data			1	3	ns
T_{off}	Rising edge of OEB to digital output tri-state			1	3	ns
T_{rD}	Data rising time ⁽⁴⁾	5 pF load, SRC = 0		2.8		ns
		5 pF load, SRC = 1		5.7		ns
T_{fD}	Data falling time ⁽⁴⁾	5 pF load, SRC = 0		2		ns
		5 pF load, SRC = 1		4.3		ns

1. See [Figure 34](#).
2. Guaranteed by design.
3. T_{dr} is linked to the duty cycle, conditioned by the duration of the low level of DR signal.
4. See [Figure 35](#) and [Figure 36](#).

Figure 11. Timing diagram



The input signal is sampled on the rising edge of the clock while the digital outputs are synchronized on the falling edge of the clock. The duty cycles on DR and CLK are the same.

6 Absolute maximum ratings and operating conditions

Table 4. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog supply voltage	3.3	V
DV_{CC}	Digital supply voltage	3.3	V
V_{CCBI}	Digital buffer supply voltage	3.3	V
V_{CCBE}	Digital buffer supply voltage	3.6	V
V_{IN} V_{INB}	Analog inputs: bottom limit → top limit	-0.6 V → $AV_{CC}+0.6$ V	V
V_{REFP} V_{INCM}	External references: bottom limit → top limit	-0.6 V → $AV_{CC}+0.6$ V	V
I_{Dout}	Digital output current	-100 to 100	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thjc}	Thermal resistance junction to case	22	°C/W
R_{thja}	Thermal resistance junction to ambient	125	°C/W
ESD	HBM (human body model) ⁽¹⁾	2	kV

1. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

Table 5. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
AV_{CC}	Analog supply voltage	2.3	2.5	2.7	V
DV_{CC}	Digital supply voltage	2.3	2.5	2.7	V
V_{CCBI}	Digital internal buffer supply	2.3	2.5	2.7	V
V_{CCBE}	Digital output buffer supply	2.3	2.5	3.4	V
V_{REFP}	Top external reference voltage	0.5		1.4	V
V_{REFM}	Bottom external reference voltage	0		0.5	V
V_{INCM}	Forced common mode voltage	0.2		1.1	V
V_{IN}	V_{IN} maximum voltage versus GND		1.6		V
	V_{IN} minimum voltage versus GND		-0.2		V
V_{INB}	V_{INB} maximum voltage versus GND		1.6		V
	V_{INB} minimum voltage versus GND		-0.2		V
DFSB	Digital inputs ⁽¹⁾	GND		V_{CCBE}	V
SRC					
OEB					

1. See [Table 9](#) for thresholds.

7 Electrical characteristics (unchanged after 300 kRad)

Unless otherwise specified, the test conditions in the following tables are:

$AV_{CC} = DV_{CC} = V_{CCBI} = V_{CCBE} = 2.5\text{ V}$, $F_S = 50\text{ Msps}$, differential input configuration,

$F_{in} = 15\text{ MHz}$, $V_{REFP} = \text{internal}$, $V_{REFM} = 0\text{ V}$, $T_{amb} = 25^\circ\text{ C}$.

Table 6. Analog inputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IN}-V_{INB}$	Full-scale input differential voltage ⁽¹⁾ (FS) ⁽²⁾			2		V _{p-p}
C_{in}	Input capacitance			7.0		pF
R_{in}	Input resistance			5		kΩ
ERB	Effective resolution bandwidth ⁽¹⁾			95		MHz

1. See [Chapter 8: Definitions of specified parameters on page 29](#) for more information.

2. Optimized differential input: 2 Vp-p. The optimized single-ended input is below 1.5 Vp-p.

Table 7. Internal reference voltage

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{REFP}	Top internal reference voltage ⁽¹⁾	$AV_{CC} = 2.5\text{ V}$	0.79	0.95	1.16	V
V_{INCM}	Input common mode voltage ⁽¹⁾	$AV_{CC} = 2.5\text{ V}$	0.40	0.52	0.67	V
TempCo	Temperature coefficient of V_{REFP} ⁽¹⁾	$T_{min} < T_{amb} < T_{max}$		0.12		mV/°C
	Temperature coefficient of V_{INCM} ⁽¹⁾	$T_{min} < T_{amb} < T_{max}$		0.12		mV/°C

1. Not fully tested over the temperature range. Guaranteed by sampling.

Table 8. Accuracy at $F_S = 50\text{ Msps}$

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
OE	Offset error	$F_{in} = 2\text{ MHz}$, $V_{IN} = 1\text{ Vp-p}$		+/-0.3		LSB
DNL	Differential non-linearity ⁽¹⁾	$F_{in} = 2\text{ MHz}$, $V_{IN} = 1\text{ Vp-p}$		+/-0.5		LSB
INL	Integral non-linearity ⁽¹⁾	$F_{in} = 2\text{ MHz}$, $V_{IN} = 1\text{ Vp-p}$		+/-1.7		LSB
-	Monotonicity and no missing codes		Guaranteed			

1. See [Chapter 8](#) for more information.

Table 9. Digital inputs and outputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Clock input						
CT	Clock threshold	$DV_{CC} = 2.5\text{ V}$		1.25		V
CA	Clock amplitude (DC component = 1.25 V)	Square clock $DV_{CC} = 2.5\text{ V}$	0.8		2.5	Vp-p
Digital inputs						
V_{IL}	Logic "0" voltage			0	$0.25 \times V_{CCBE}$	V
V_{IH}	Logic "1" voltage		$0.75 \times V_{CCBE}$	V_{CCBE}		V
Digital outputs						
V_{OL}	Logic "0" voltage	$I_{OL} = -1\text{ mA}$		0	0.2	V
V_{OH}	Logic "1" voltage	$I_{OH} = 1\text{ mA}$	$V_{CCBE} - 0.2\text{ V}$			V
I_{OZ}	High impedance leakage current	OEB set to V_{IH}	-15		15	μA

Table 10. Dynamic characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SFDR	Spurious free dynamic range	$F_{in} = 15\text{ MHz}$		-75	-63	dBc
		$F_{in} = 95\text{ MHz}$		-70		
		$F_{in} = 145\text{ MHz}$		-57		dBc
SNR	Signal to noise ratio	$F_{in} = 15\text{ MHz}$	59	63		dB
		$F_{in} = 95\text{ MHz}$		60		dB
		$F_{in} = 145\text{ MHz}$		59		
THD	Total harmonics distortion	$F_{in} = 15\text{ MHz}$		-76	-64	dB
		$F_{in} = 95\text{ MHz}$		-72		dB
		$F_{in} = 145\text{ MHz}$		-58		
SINAD	Signal to noise and distortion ratio	$F_{in} = 15\text{ MHz}$	58	63		dB
		$F_{in} = 95\text{ MHz}$		60		
		$F_{in} = 145\text{ MHz}$		56.5		dB
ENOB	Effective number of bits	$F_{in} = 15\text{ MHz}$	9.7	10.3		bits
		$F_{in} = 95\text{ MHz}$		9.5		bits
		$F_{in} = 145\text{ MHz}$		9.1		
PSRR	Power supply rejection ratio	$F = 260\text{ kHz}$ $F_s = 2\text{ MHz}$ $R_{pol} = 200\text{ k}\Omega$ each power supply at 2.5 V decoupled by $10\text{ }\mu\text{F}/470\text{ nF}$		93		dB

Figure 12. Differential input configuration

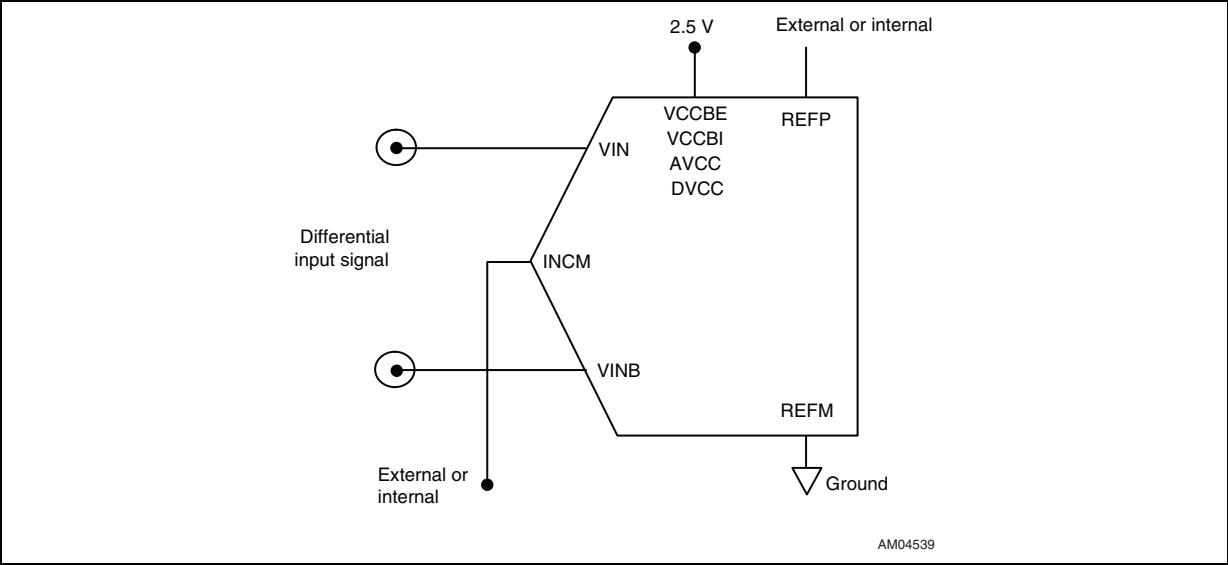


Figure 13. ENOB vs. diff. input, square clock

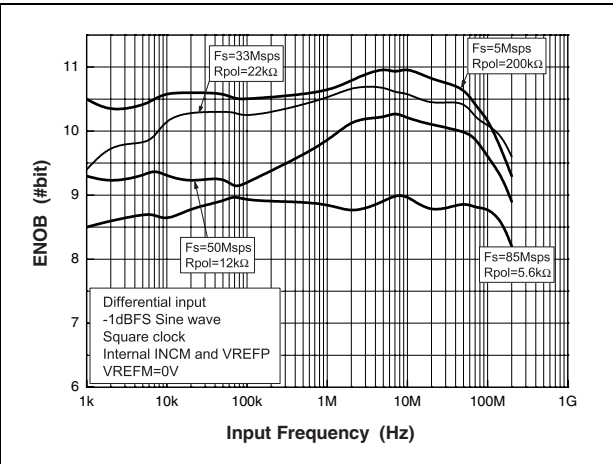


Figure 14. SINAD vs. diff. input, square clock

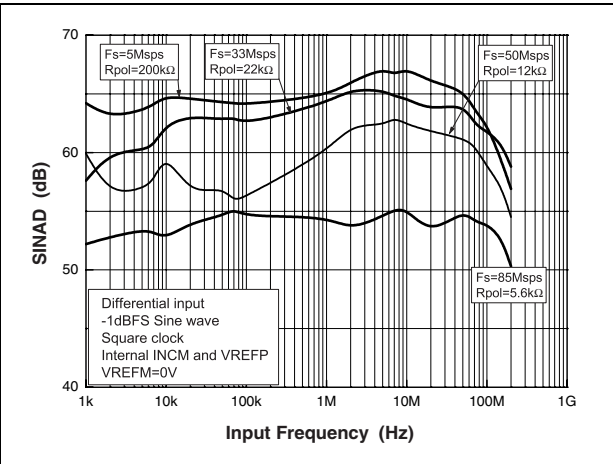


Figure 15. THD vs. diff. input, square clock

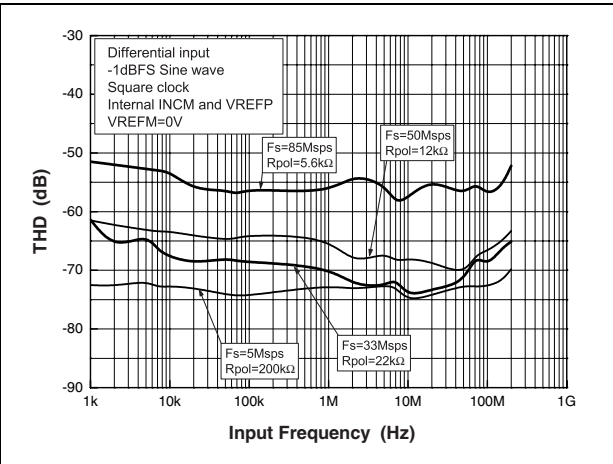


Figure 16. SNR vs. diff. input, square clock

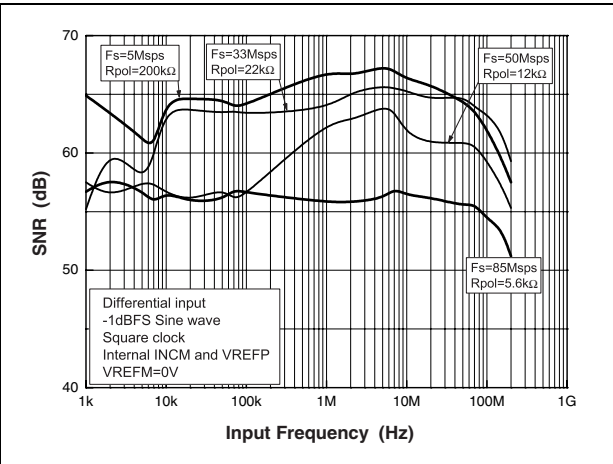


Figure 17. SFDR vs. diff. input, square clock

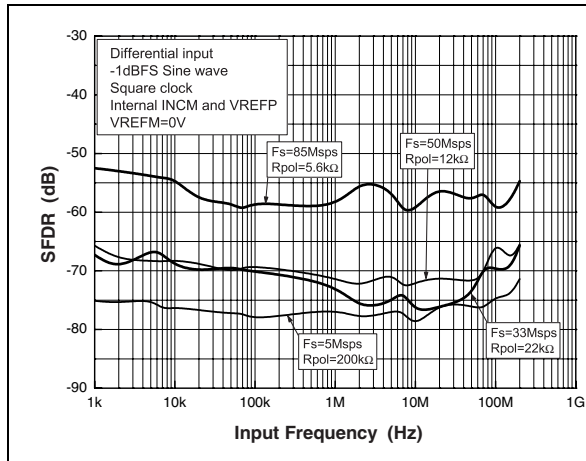


Figure 18. ENOB vs. diff. input, sine clock

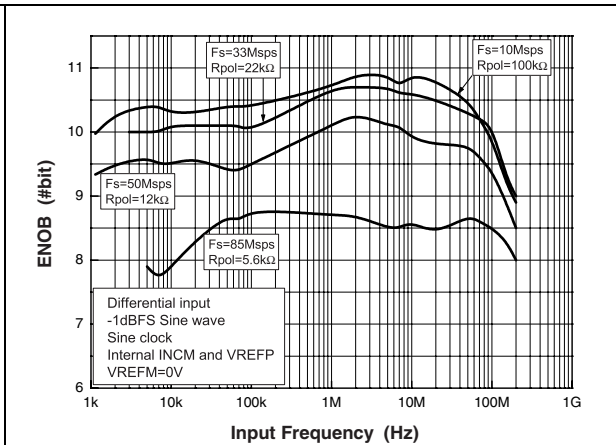


Figure 19. SINAD vs. diff. input, sine clock

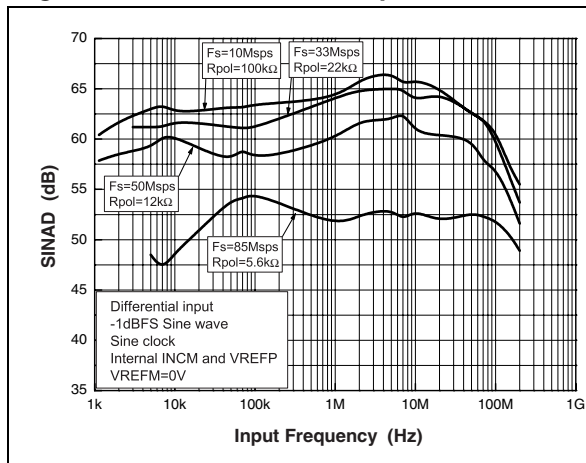


Figure 20. THD vs. diff. input, sine clock

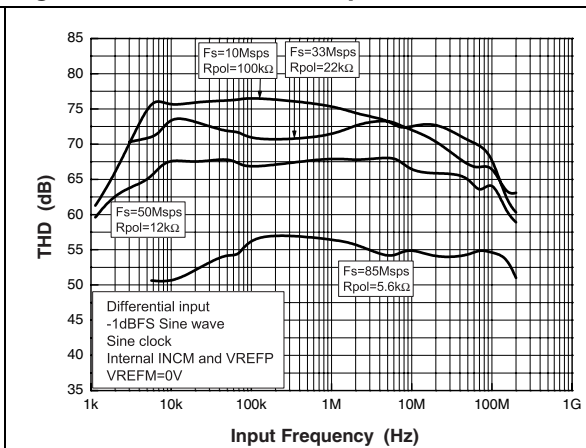


Figure 21. SNR vs. diff. input, sine clock

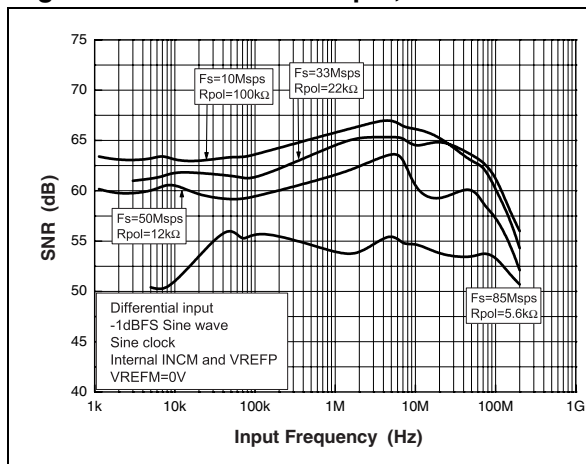


Figure 22. SFDR vs. diff. input, sine clock

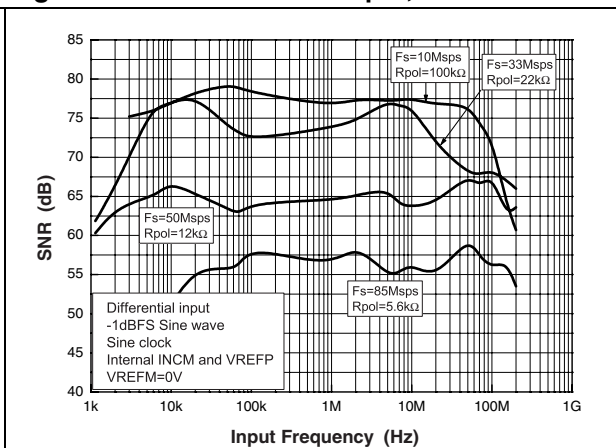


Figure 23. ENOB vs. square clock, diff. input

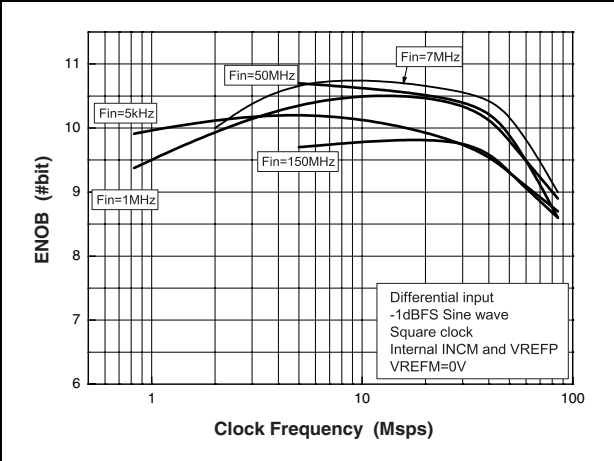


Figure 24. SINAD vs. square clock, diff. input

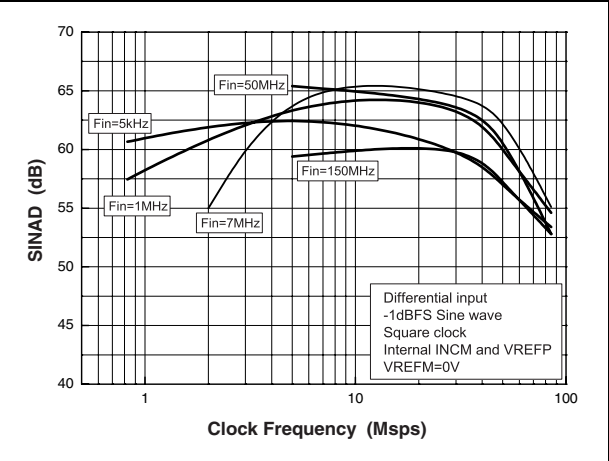


Figure 25. THD vs. square clock, diff. input

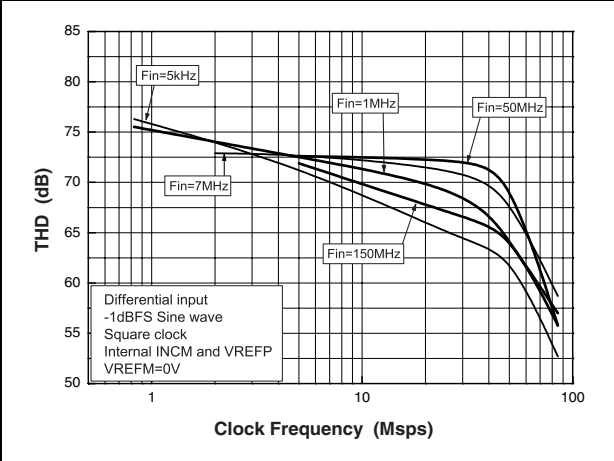


Figure 26. SNR vs. square clock, diff. input

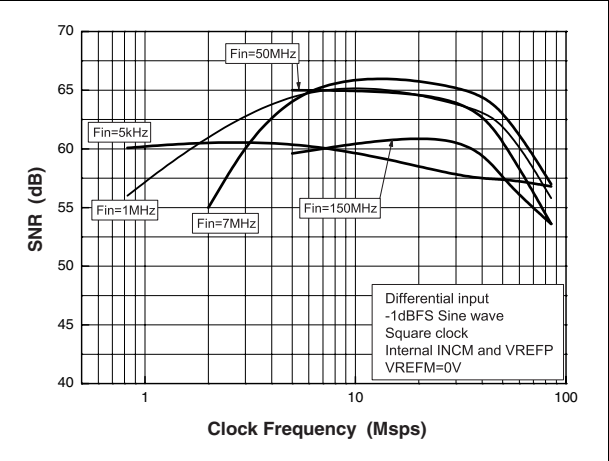


Figure 27. SFDR vs. square clock, diff. input

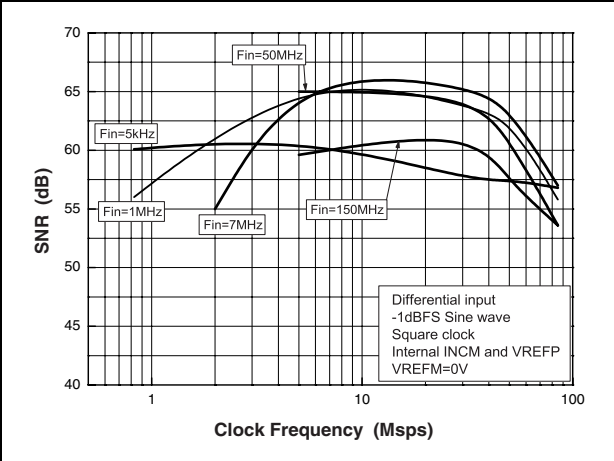


Figure 28. ENOB vs. sine clock, diff. input

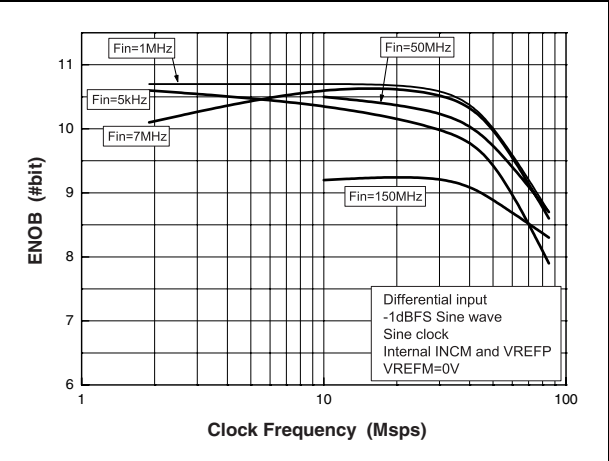


Figure 29. SINAD vs. sine clock, diff. input

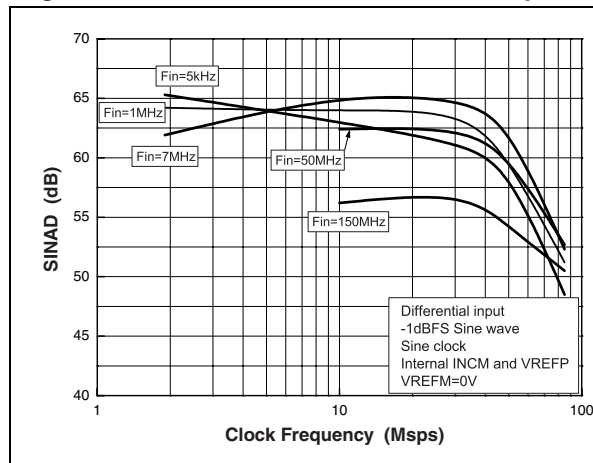


Figure 30. THD vs. sine clock, diff. input

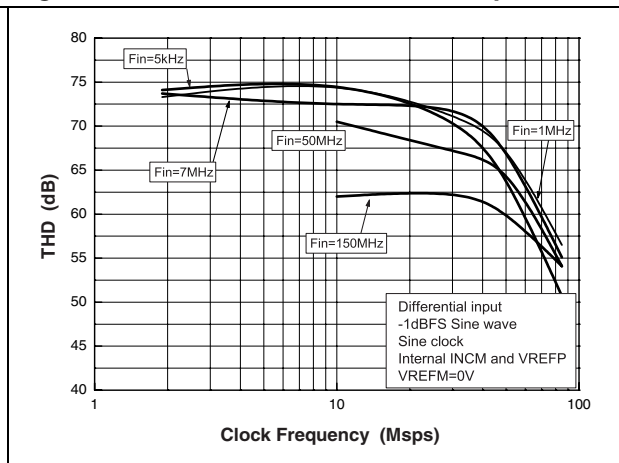


Figure 31. SNR vs. sine clock, diff. input

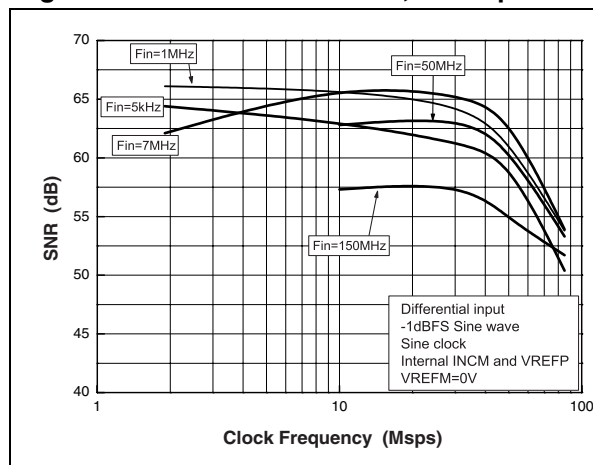


Figure 32. SFDR vs. sine clock, diff. input

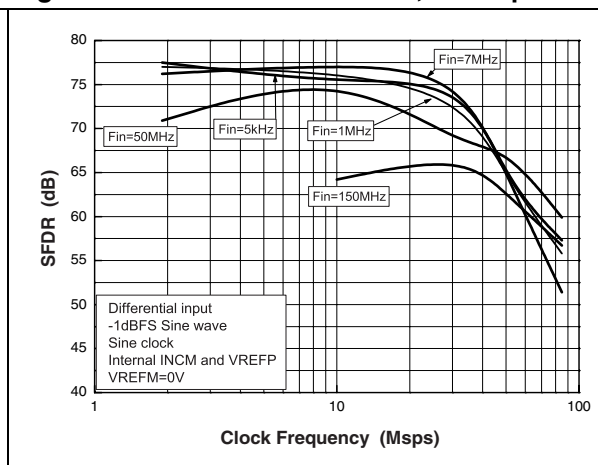


Figure 33. Clock threshold vs. temperature

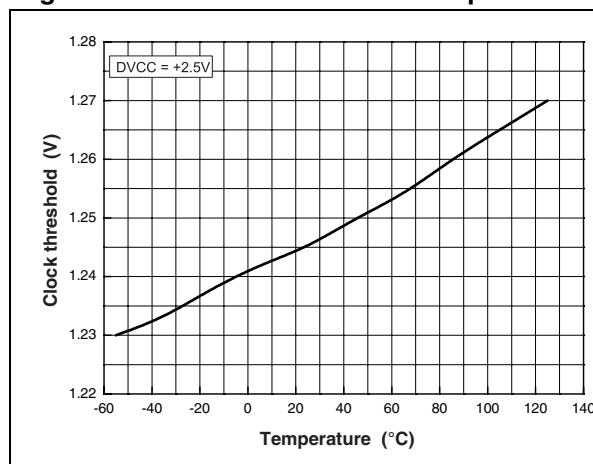


Figure 34. ENOB vs. clock duty cycle

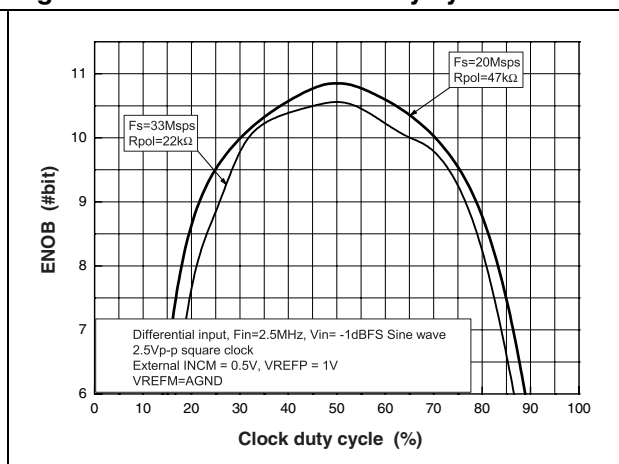


Figure 35. Output buffer fall time

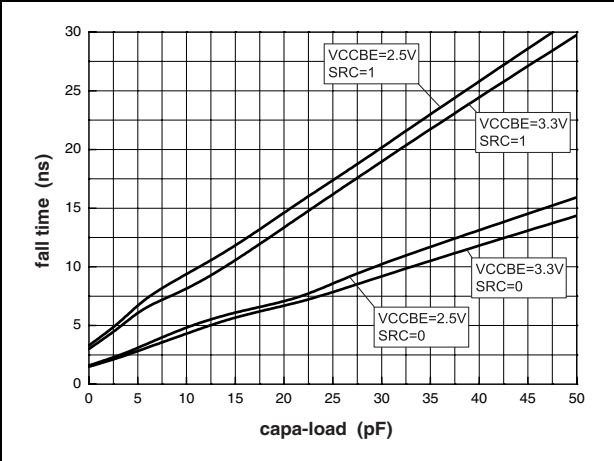


Figure 36. Output buffer rise time

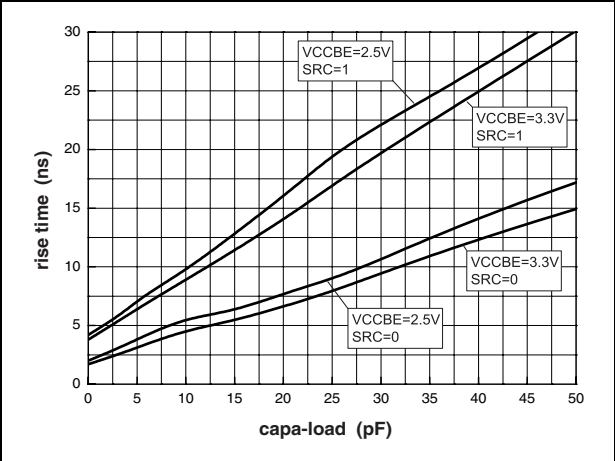


Figure 37. Single-ended input configuration

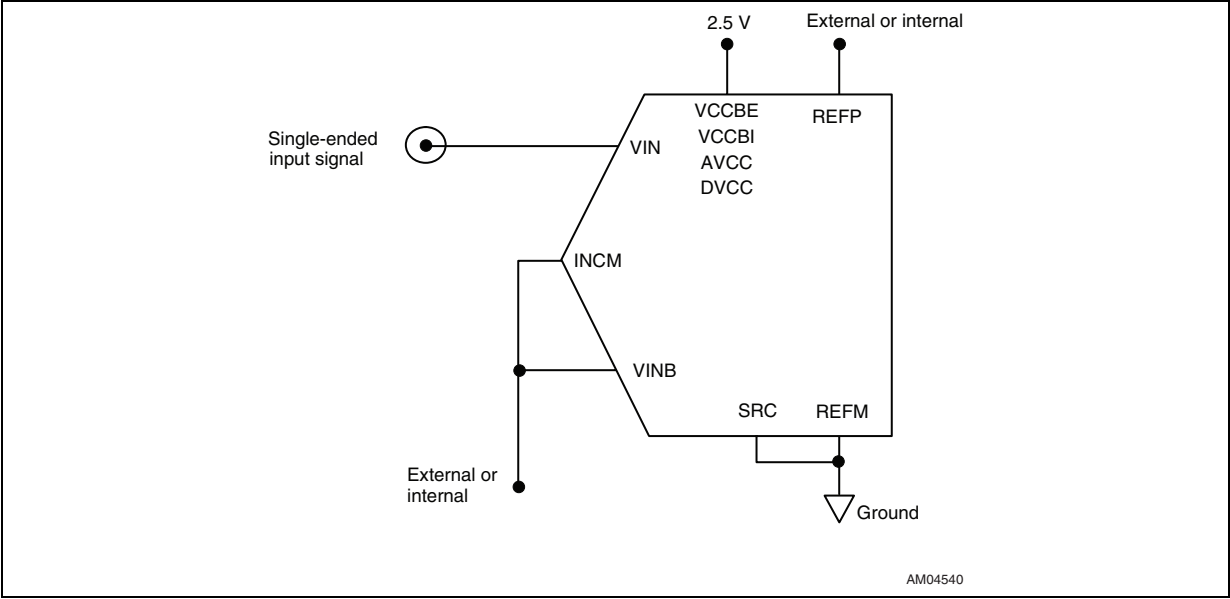


Figure 38. ENOB vs. Fin, single-ended

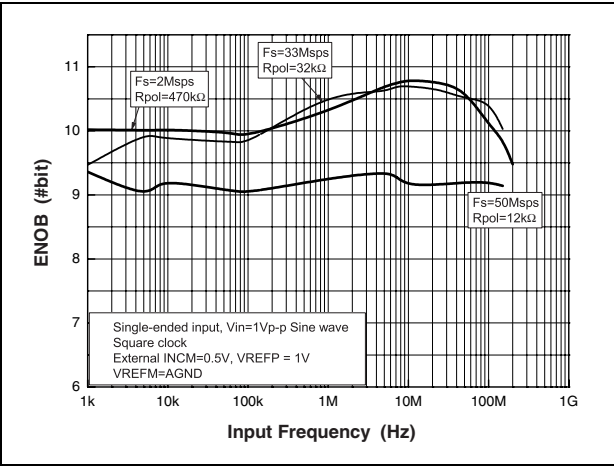


Figure 39. SINAD vs. Fin, single-ended

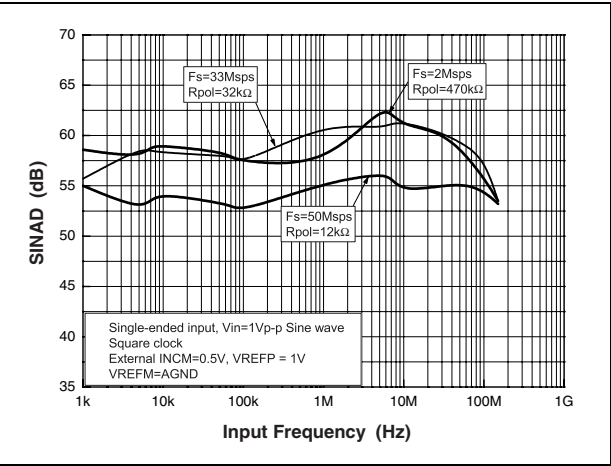


Figure 40. THD vs. Fin, single-ended

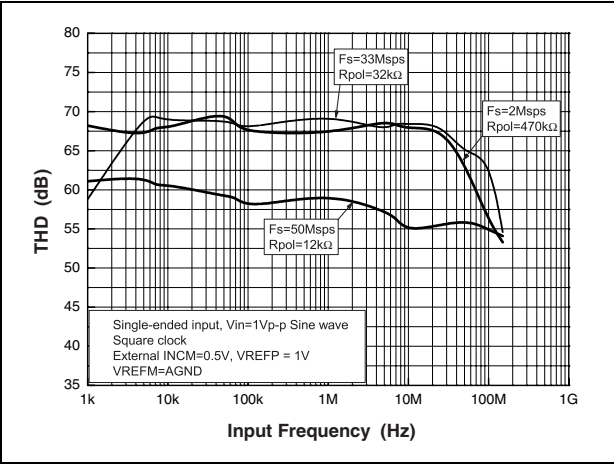


Figure 41. SNR vs. Fin, single-ended

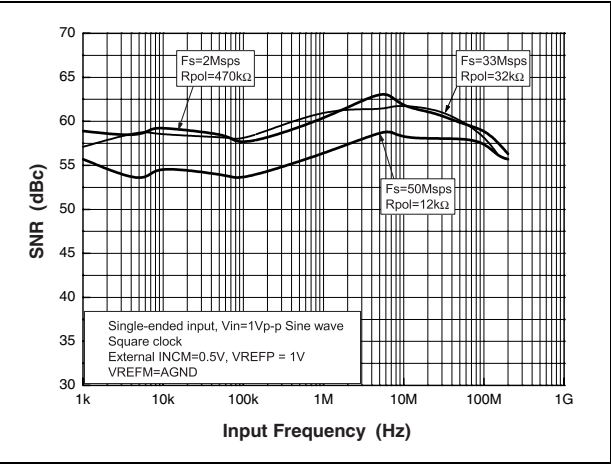


Figure 42. SFDR vs. Fin, single-ended

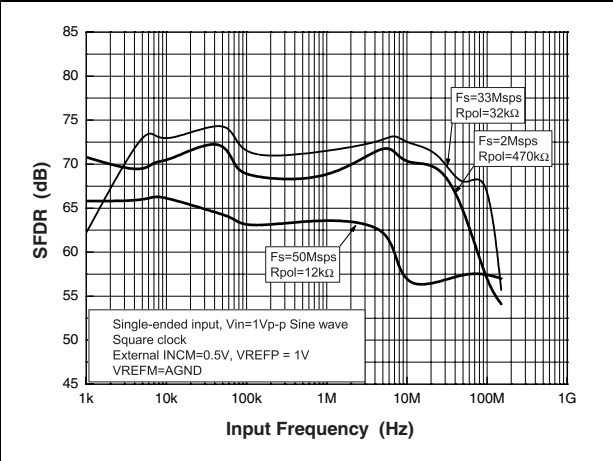


Figure 43. ENOB vs. Vin, single-ended

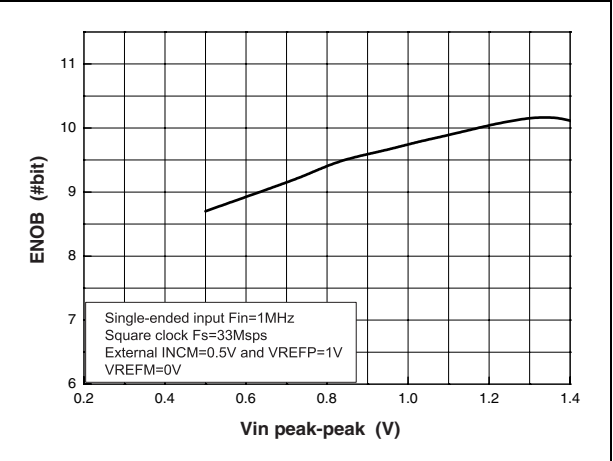


Figure 44. ENOB vs. INCM, single-ended

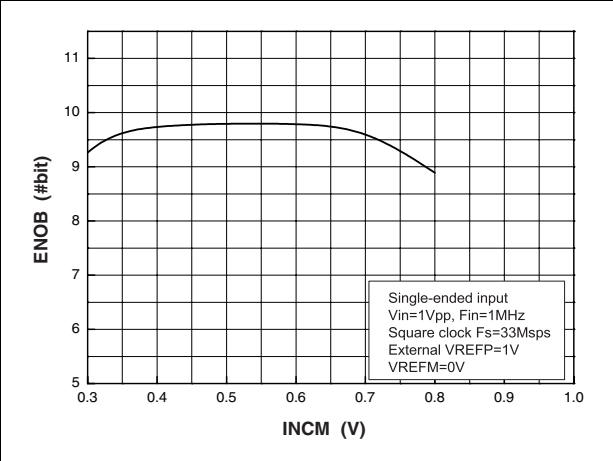
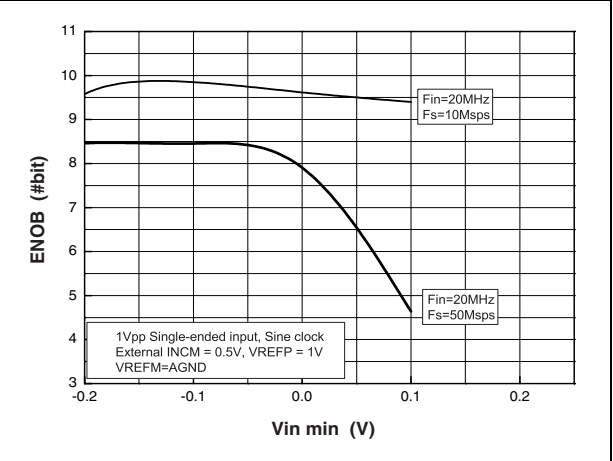


Figure 45. ENOB vs. Vin min, single-ended



7.1 RHF1201 operating modes

Extra functionalities are provided to simplify the application board as much as possible. The operating modes offered by the RHF1201 are described in [Table 11](#).

Table 11. RHF1201 operating modes

Inputs				Outputs		
Analog input differential amplitude	DFSB	OEB	SRC	OR	DR	Most significant bit (MSB)
$(V_{IN}-V_{INB})$ above maximum range	H	L	X	H	CLK	D11
	L	L	X	H	CLK	D11 complemented
$(V_{IN}-V_{INB})$ below minimum range	H	L	X	H	CLK	D11
	L	L	X	H	CLK	D11 complemented
$(V_{IN}-V_{INB})$ within range	H	L	X	L	CLK	D11
	L	L	X	L	CLK	D11 complemented
X	X	H	X	High Impedance		
X	X	L	H	X	CLK low slew rate	Low slew rate
X	X	L	L	X	CLK high slew rate	High slew rate

7.1.1 Inputs

Data format select (DFSB): when set to low level (V_{IL}), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing some further signal processing. When set to high level (V_{IH}), DFSB provides a standard binary output coding.

Output enable (OEB): when set to low level (V_{IL}), all digital outputs remain active. When set to high level (V_{IH}), all digital output buffers are in high impedance state while the converter goes on sampling. When OEB is set to a low level again, the data arrives on the output with a very short T_{on} delay. This feature enables the chip select of the device. [Figure 11 on page 8](#) summarizes this functionality.

Slew rate control (SRC): when set to high level (V_{IH}), all digital output currents are limited to a clamp value so that any digital noise power is reduced to the minimum. When set to low level (V_{IL}), the output edges are twice as fast.

7.1.2 Outputs

Out-of-range (OR): this function is implemented at the output stage to automatically detect any digital data that is over the full-scale range. For data within the range, OR remains in a low-level state (V_{OL}), but switches to a high-level state (V_{OH}) as soon as out-of-range data is detected.

Data ready (DR): the data ready output is an image of the clock being synchronized on the output data (D0 to D11). This is a very helpful signal that simplifies the synchronization of the measurement equipment or of the controlling DSP.

As all other digital outputs, DR and OR go into a high impedance state when OEB is set to high level, as shown in [Figure 11 on page 8](#).

7.2 Driving the analog input

Figure 46. Equivalent VIN - VINB (differential input)

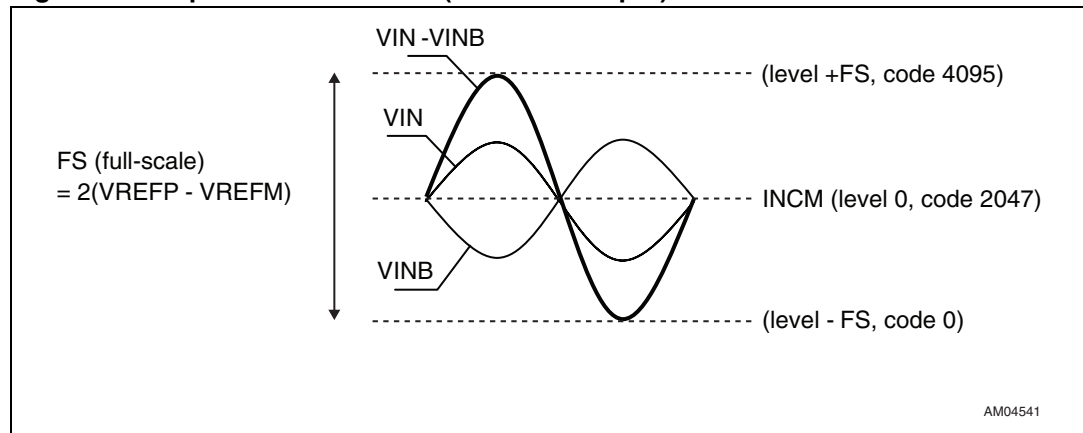


Figure 47. Maximum input swing on each VIN or VINB input

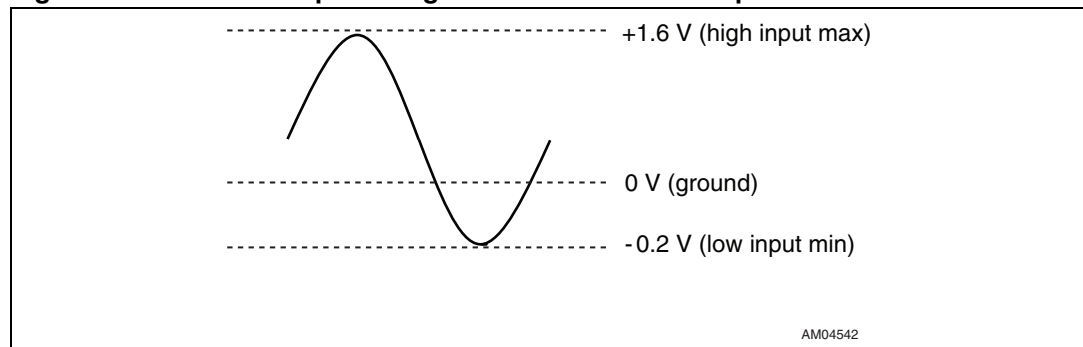
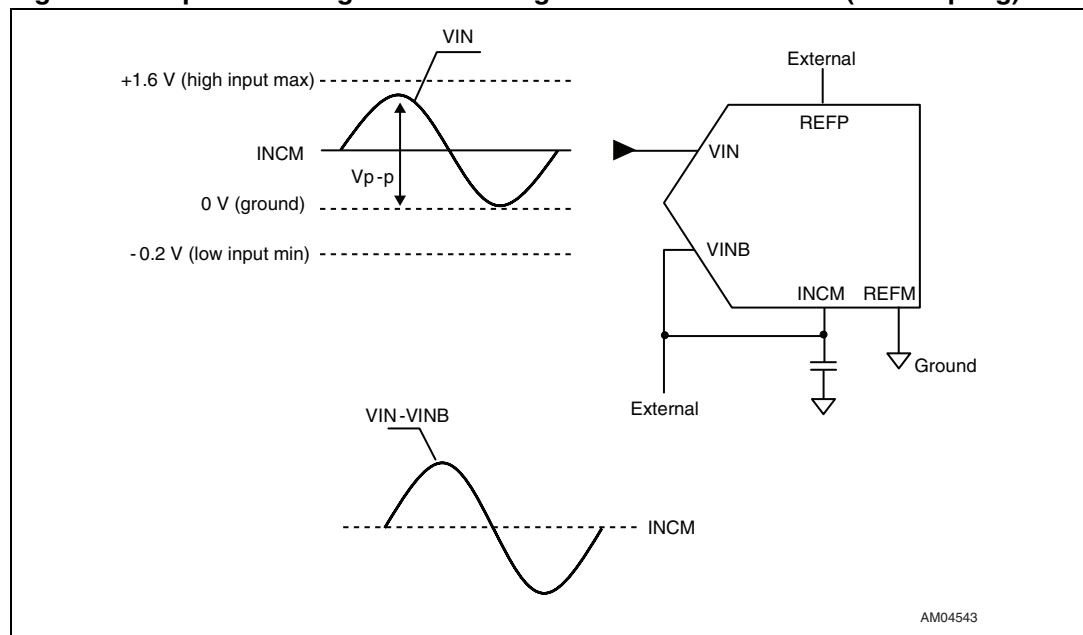
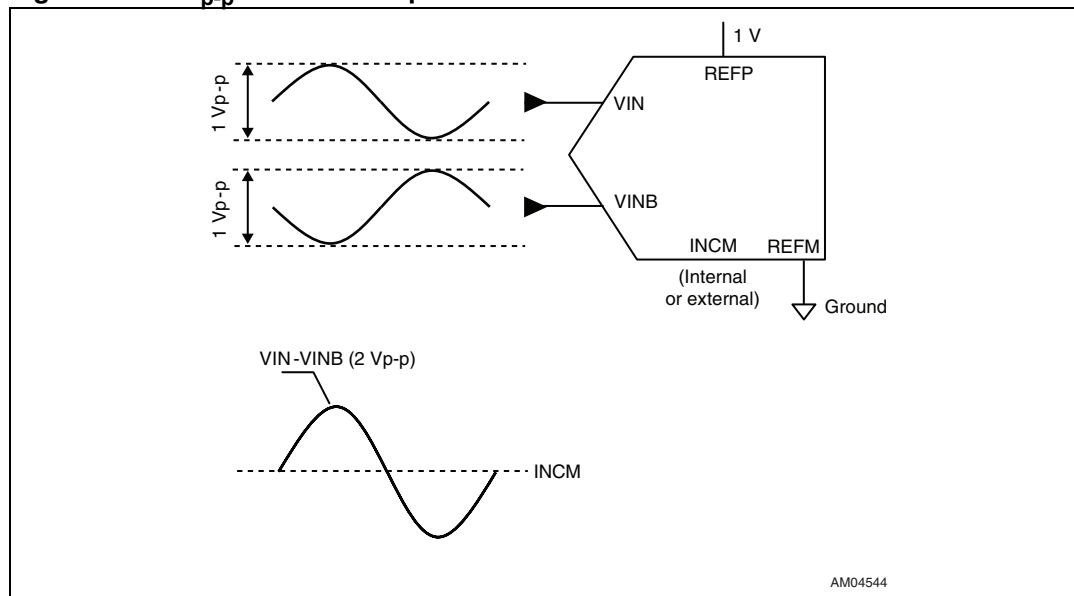


Figure 48. Optimized single-ended configuration at VREFP = 1 V (DC coupling)



The RHF1201 is designed for use in a differential input configuration. Nevertheless, it can achieve good performance in a single-ended input configuration. In single-ended, a good-quality conversion can be achieved by using an input amplitude up to 1.4 V_{p-p} with external references INCM and VREFP (see [Figure 38 on page 17](#)).

Figure 49. 2 V_{p-p} differential input

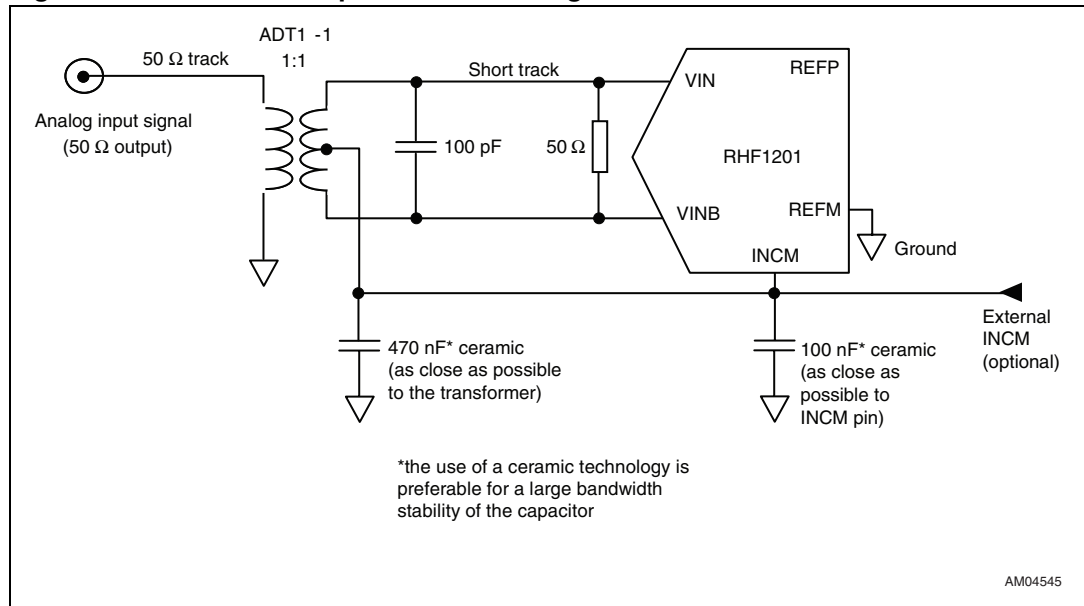
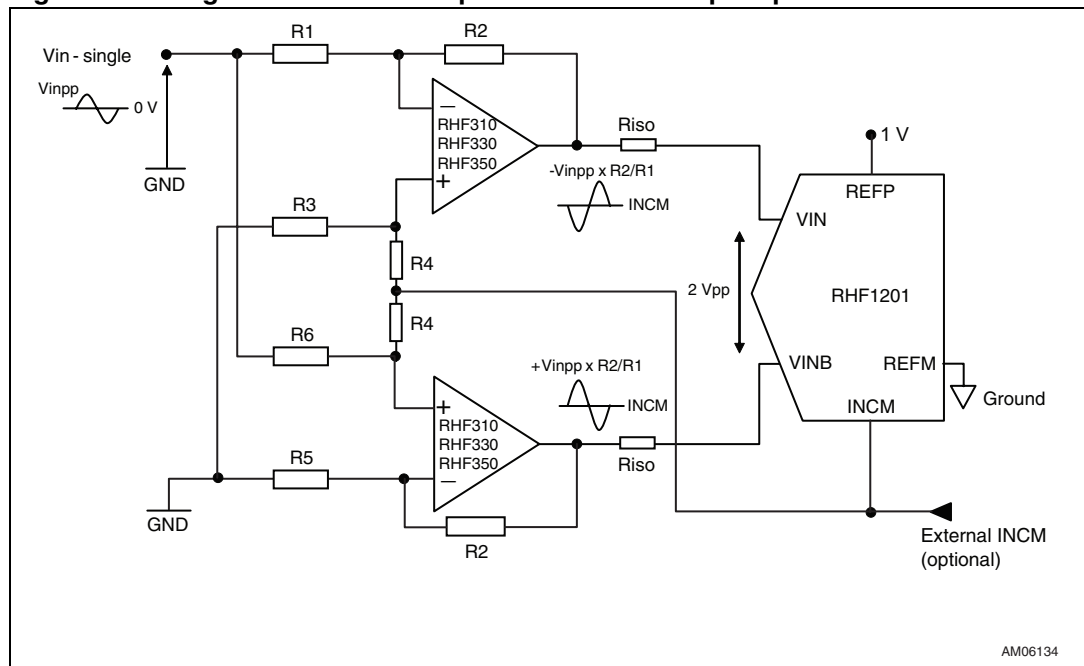


The RHF1201 is designed to obtain optimum performance when driven on differential inputs with a differential amplitude of 2 V peak-to-peak (2 V_{p-p}). This is the result of 1 V_{p-p} on the VIN and VINB inputs in phase opposition.

The RHF1201 is specifically designed to meet sampling requirements for IF, intermediate frequency input signals. In particular, the track-and-hold in the first stage of the pipeline is designed to minimize the linearity limitations as the analog frequency increases. This is achieved by making the input impedance independent of the input frequency.

[Figure 50 on page 23](#) shows a differential input solution. The input signal is fed to the transformer's primary, while the secondary drives both ADC inputs. The transformer must be 50 Ω matched (for proper matching with a 50 Ω generator), and it must be loaded with 50 Ω on the secondary, as close as the ADC. Tracks between the secondary and VIN and VINB pins must be as short as possible.

The common mode voltage of the ADC (INCM) is connected to the center tap of the transformer's secondary in order to bias the input signal around this common voltage, internally set to 0.52 V (see [Table 7 on page 10](#)). The INCM is decoupled to maintain a low noise level on this node. Ceramic technology for decoupling provides good capacitor stability across a wide bandwidth.

Figure 50. Differential implementation using a balun**Figure 51. Single-to-differential implementation with op-amps**

With $(V_{out-diff}) = (2R_2/R_1) \times (V_{in-single})$ and the following conditions on resistors:
 $R_1/(R_1+R_2) = R_3/(R_3+R_4)$ and $R_4/(R_6+R_4) = (R_5+R_2)/R_1$ (refer to the RHF310-330-350 datasheet for the choice of R_2).

Some applications may require a single-ended input, which can easily be achieved with the configuration shown in [Figure 52](#). However, with this type of configuration a degradation in the rated performance of the RHF1201 may occur, compared to a differential configuration. To avoid this, a sufficiently decoupled DC reference should be used to bias the RHF1201 inputs. One may also use an AC-coupled analog input and set the DC analog level with a high value resistor R (10 kΩ to 100 kΩ) connected to a proper DC source.

C_{in} and R behave like a high-pass filter and are calculated to set the lowest possible cut-off frequency. An example of VINB decoupling to reduce noise is shown in [Figure 52](#).

Figure 52. AC-coupling single-ended input configuration

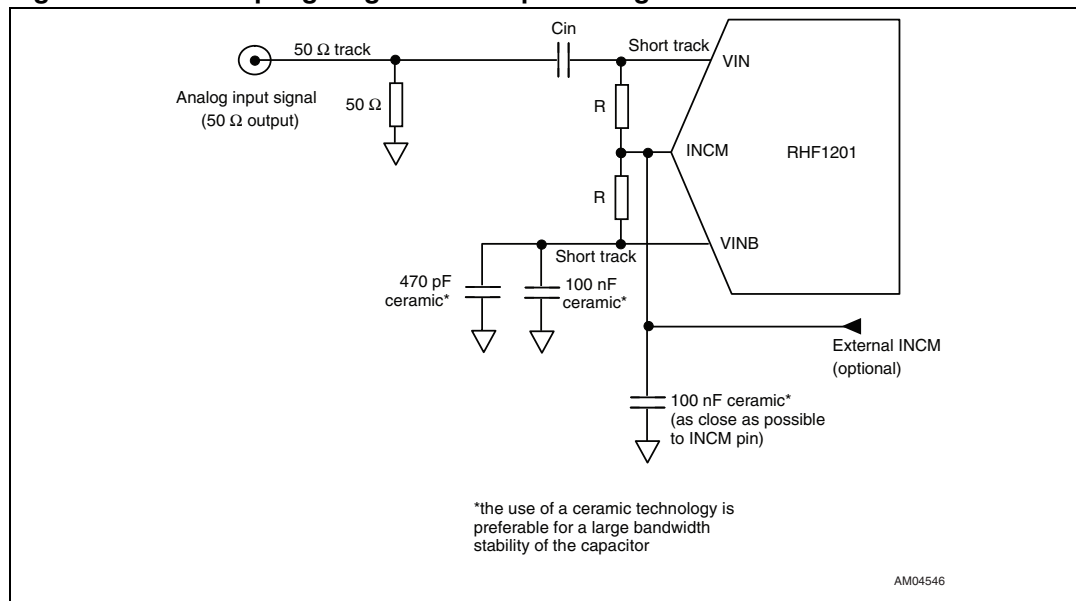
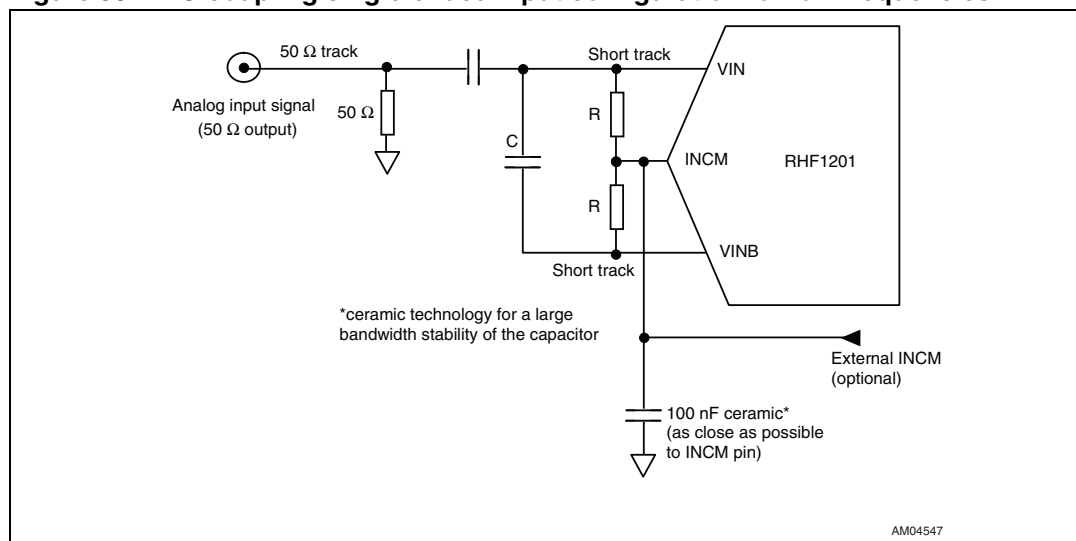


Figure 53. AC-coupling single-ended input configuration for low frequencies



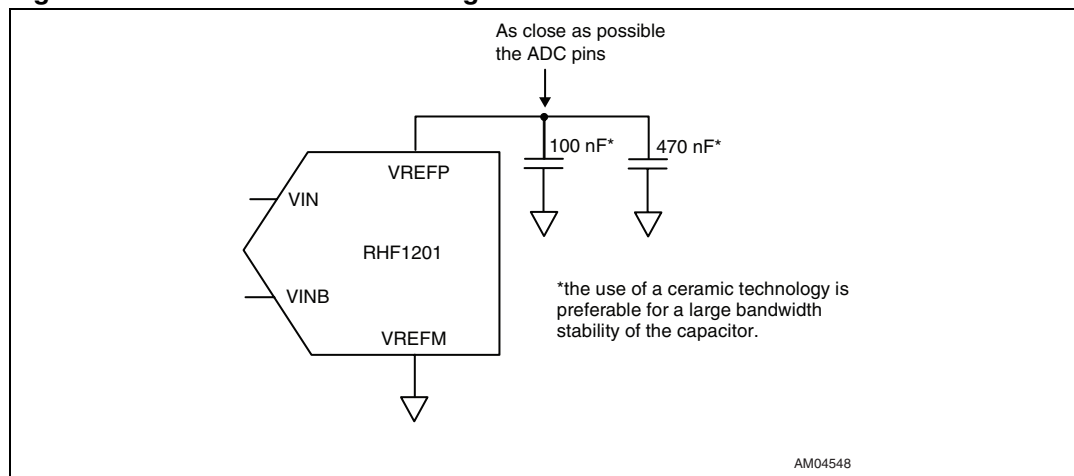
The C capacitor (in the range of 33 pF for example) is dedicated to a low input frequency range. This capacitor is efficient in reducing noise at higher frequencies. When coupled with the resistors, R and C together behave like a high-pass filter. For example, if $R = 10\text{ k}$ and $C = 33\text{ pF}$, the cut-off frequency of this filter equals 482 kHz.

7.3 Reference connection

7.3.1 Internal reference

In the standard configuration, the ADC is biased with the internal reference voltage. The V_{REFM} pin is connected to analog ground while V_{REFP} is internally set to a voltage close to 1.0 V. V_{REFP} should be decoupled so as to minimize low and high frequency noise. [Figure 54](#) shows the schematics.

Figure 54. Internal reference setting



7.3.2 External reference

An external reference voltage can be used for specific applications requiring even better linearity or enhanced temperature behavior. In such cases, the amplitude of the external voltage must be at least equal to the internal reference (see [Table 7: Internal reference voltage on page 10](#)). An external voltage reference with the configuration shown in [Figure 55](#) and [Figure 56](#) can be used to obtain optimum performance. Decoupling is achieved by using ceramic capacitors, which provide optimum linearity versus frequency.

Figure 55. External reference setting

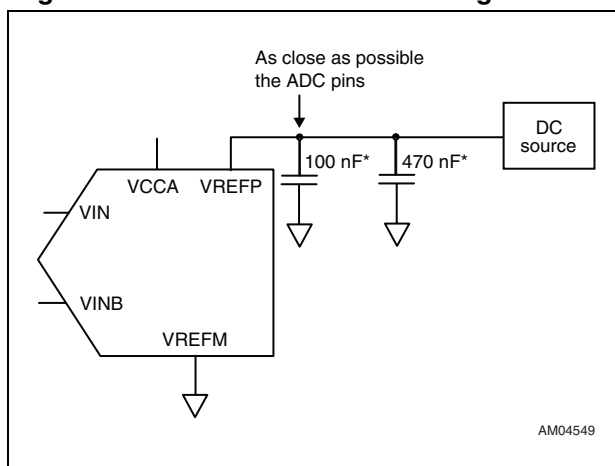
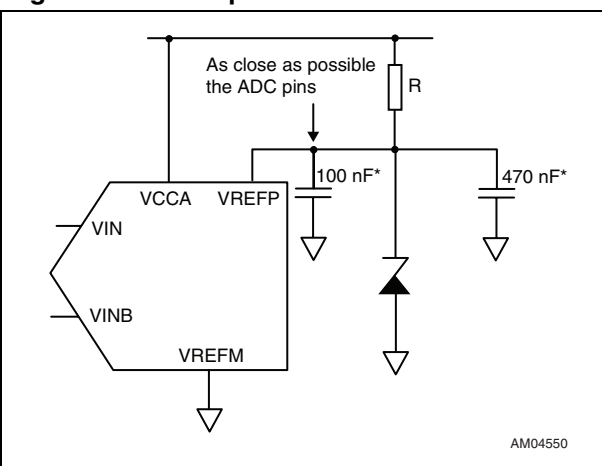


Figure 56. Example with a zener



Note: * The use of ceramic technology is preferable for large bandwidth stability of the capacitor.

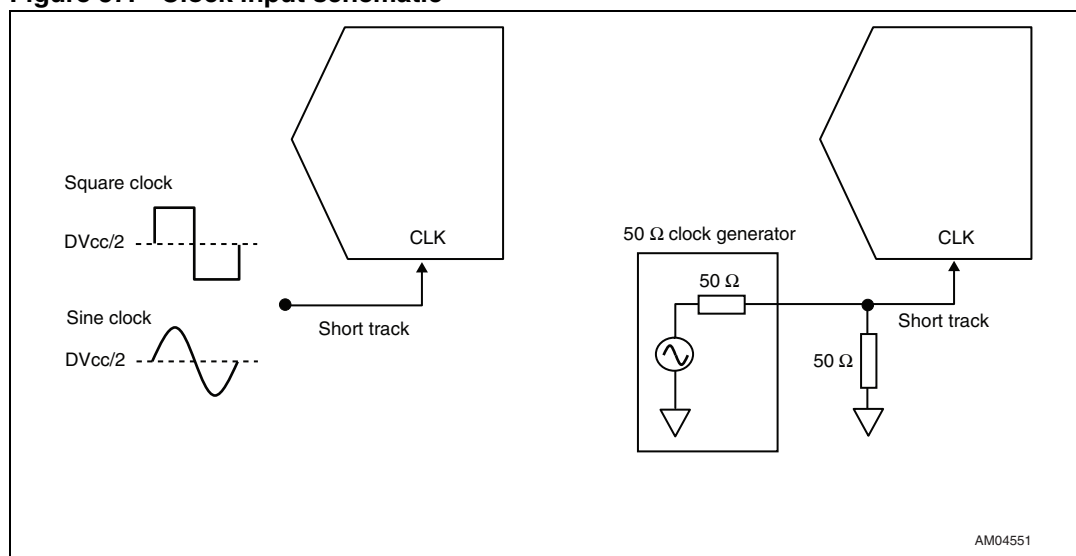
7.4 Clock input

The quality of the converter very much depends on the accuracy of the clock input in terms of jitter. The use of a low jitter, crystal-controlled oscillator is recommended.

The following points should also be considered.

- At 45 Msps, the duty cycle must be between 45% and 65%.
- The clock power supplies must be independent of the ADC output supplies to avoid digital noise modulation on the output.
- When powered-on, the circuit needs several clock periods to reach its normal operating conditions.
- The clock input is a MOS input. To bias this input stage properly, a bias current of 10 nA is sufficient.

Figure 57. Clock input schematic



The signal applied to the CLK pin is critical to obtain full performance from the RHF1201. We recommend using a 0 to 2.5 V square signal with fast transition times, and to place proper termination resistors as close as possible to the device.

The sampling instant is determined by the rising edge of the clock signal. The jitter associated with this instant must be as low as possible to avoid SNR degradation on fast-moving input signals. To ensure that LSB errors stay below 0.5, the total jitter T_j must satisfy the following condition for a full-scale input signal.

$$T_j < \frac{1}{\pi \cdot F_{in} \cdot 2^{n+1}}$$

n being the number of bits.

In most cases, the clock signal jitter is the major contributor of total noise. Therefore, particular attention should be given to the clock signal when acquiring fast signals with a low-frequency clock.

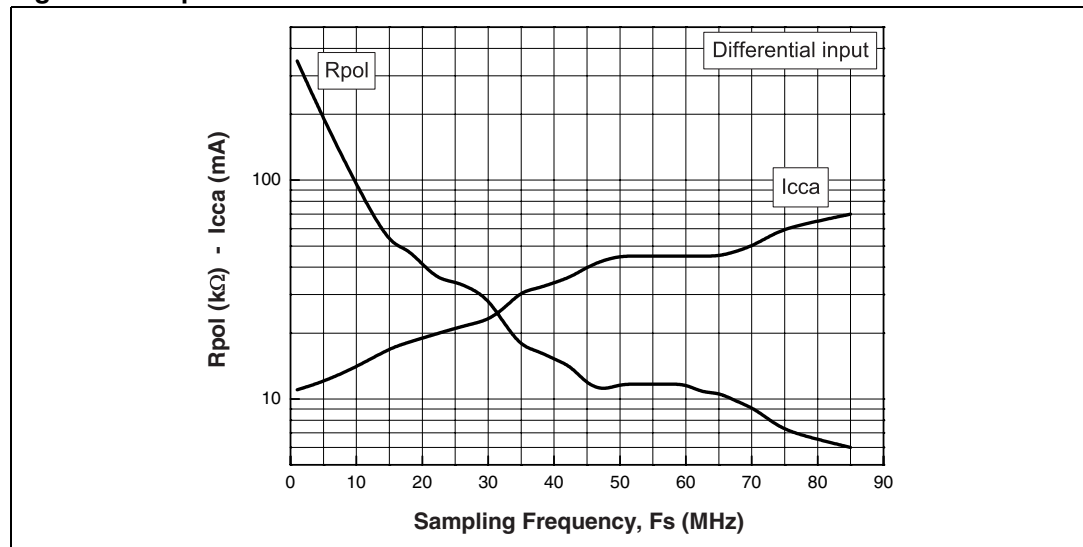
7.5 Power consumption optimization

The internal architecture of the RHF1201 makes it possible to optimize the power consumption according to the sampling frequency of the application. For this purpose, an external R_{pol} resistor is placed between the IPOL pin and the analog ground. Therefore, the total dissipation can be adjusted across the entire sampling range from 0.5 Msps to 50 Msps to fulfill the requirements of applications where power saving is critical.

For low sampling frequencies, the resistor value may be adjusted to decrease the analog current without any deterioration of the dynamic performance.

The current consumption I_{cca} , depending on the value of R_{pol} , is as shown in [Figure 58](#).

Figure 58. R_{pol} versus F_s



7.6 Layout precautions

- Use of dedicated analog and digital ground planes on the PCB is recommended for high-speed circuit applications to provide low parasitic inductance and resistance. Ground planes under the digital pins and layers should be avoided to minimize parasitic capacitances.
- The separation of the analog signal from the digital output is mandatory to prevent noise from coupling onto the input signal.
- Power supply bypass capacitors must be placed as close as possible to the IC pins to improve high-frequency bypassing and reduce harmonic distortion.
- All leads must be as short as possible, especially for the analog input, so as to decrease parasitic capacitance and inductance.
- To minimize the transition current when the output changes, the capacitive load at the digital outputs must be reduced as much as possible by using the shortest-possible routing tracks.
- Choose the smallest-possible component sizes (SMD).

8 Definitions of specified parameters

8.1 Static parameters

Differential non-linearity (DNL)

The average deviation of any output code width from the ideal code width of 1 LSB.

Integral non-linearity (INL)

An ideal converter exhibits a transfer function which is a straight line from the starting code to the ending code. The INL is the deviation from this ideal line for each transition.

8.2 Dynamic parameters

Spurious free dynamic range (SFDR)

The ratio between the power of the worst spurious signal (not always a harmonic) and the amplitude of the fundamental tone (signal power) over the full Nyquist band. Expressed in dBc.

Total harmonic distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. Expressed in dB.

Signal to noise ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($f_s/2$) excluding DC, fundamental and the first five harmonics. SNR is reported in dB.

Signal to noise and distortion ratio (SINAD)

Similar ratio as for SNR but including the harmonic distortion components in the noise figure (not DC signal). Expressed in dB.

The effective number of bits (ENOB) is easily deduced from the SINAD, using the formula:

$$\text{SINAD} = 6.02 \times \text{ENOB} + 1.76 \text{ dB}$$

When the applied signal is not full-scale (FS) but has an amplitude A_0 , the SINAD expression becomes:

$$\text{SINAD} = 6.02 \times \text{ENOB} + 1.76 \text{ dB} + 20 \log (A_0/\text{FS})$$

ENOB is expressed in bits.

Effective resolution bandwidth

For a given sampling rate and clock jitter, this is the analog input frequency at which the SINAD is reduced by 3 dB, and the ENOB is reduced by 0.5 bits.

Pipeline delay

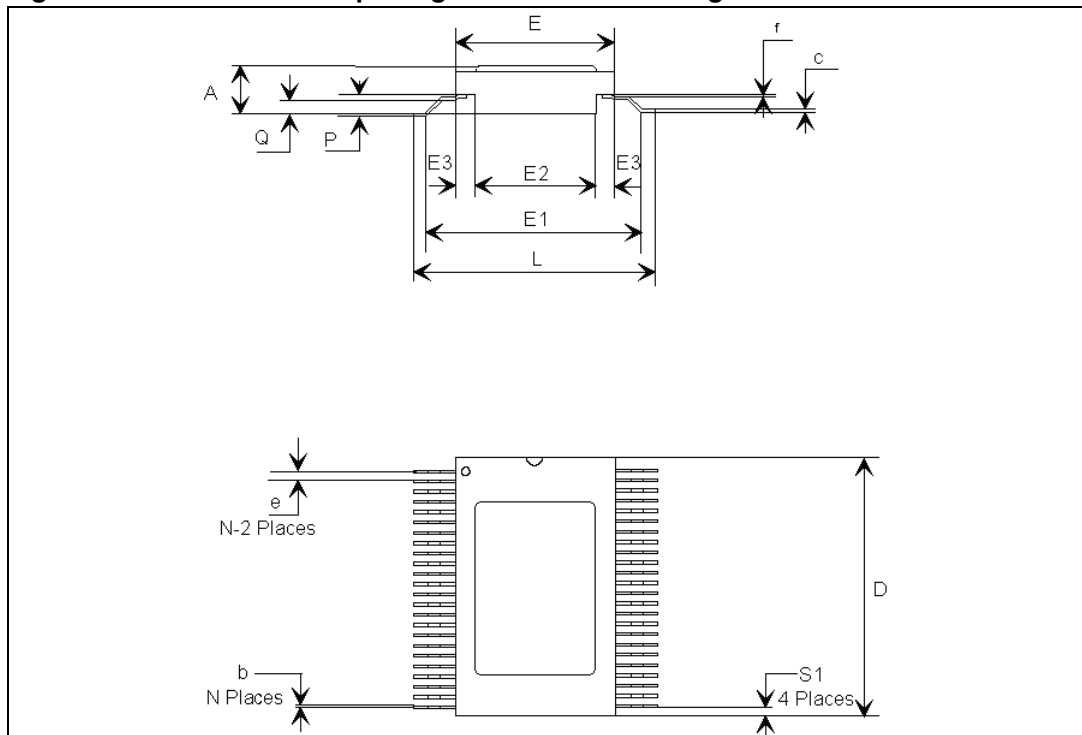
Delay between the initial sample of the analog input and the availability of the corresponding digital data output on the output bus. Also called data latency, it is expressed as a number of clock cycles.

When powering *off* to *on*, there is a delay of several clock cycles before the ADC can achieve a reliable and stable signal conversion. During this delay, some conversion artefacts may appear.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 59. Ceramic SO-48 package mechanical drawing



Note: The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

Table 12. Ceramic SO-48 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E1		10.90			0.429	
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	12.28	12.58	12.88	0.483	0.495	0.507
P	1.30	1.45	1.60	0.051	0.057	0.063
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

10 Revision history

Table 13. Document revision history

Date	Revision	Changes
01-Sep-2006	1	Initial release in new format.
29-Jun-2007	2	Updated failure immune and latchup immune value to 120 MeV-cm ² /mg. Updated package mechanical data. Removed reference to non rad-hard components from Section 7.3.2: External reference on page 25 .
10-Oct-2008	3	Changed cover page graphic. Changed Figure 2 . Added Chapter 4: Equivalent circuits . Added Note 1 under Table 4 . Expanded Table 5 with additional parameters. Modified "Test conditions" and Vrefp/Vincm in Table 7 . Improved readability in Table 11 . Added Figure 46 to Figure 49 . Modified Figure 50 and Figure 52 . Added Figure 53 . Removed <i>IF sampling</i> section. Modified Figure 54 and Figure 16 . Added Figure 58 . Added ECOPACK information and updated presentation in Chapter 9 .
09-Apr-2010	4	Modified description on cover page. Added Table 1: Device summary on page 1 . Removed RHF1201KSO2 order code from Table 1 . Removed Fs and Tck values from Table 3 . Added Figure 7 and Figure 8 . Added DFS, OEB and SRC values in Table 5 . Changed VINCM values in Table 5 . Removed Fin values from Table 5 . Removed output capacitive load values from Table 9 . Changed clock threshold values in Table 9 . Added PSRR values in Table 10 . Added Figure 13 on page 12 to Figure 45 . Modified Figure 46 , Figure 48 and Figure 49 .
29-Jul-2011	5	Added Note: on page 31 and in the "Pin connections" diagram on the coverpage.

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